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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/988,416	11/16/2001	Martin Thomas Miller	455610-2420	8540

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EXAMINER	
WEST, JEFFREY R	
ART UNIT	PAPER NUMBER
2857	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/988,416	MILLER ET AL.	
	Examiner	Art Unit	
	Jeffrey R. West	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-6,11,13,23-27,32 and 43-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-6,11,13,23-27,32 and 43-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 27, 2007, has been entered.

Claim Objections

3. Claims 23-27 and 32 are objected to because of the following informalities:

In claims 23-27 and 32, line 1, to avoid problems of antecedent basis, "The processing web" should be ---The graphical processing web---.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 2-6, 11, 23-27, 32, and 43-49 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,809,189 to Batson.

With respect to claim 43, Batson discloses a method for configuring and performing processing in a digital oscilloscope processing apparatus (column 2, lines 13-14), comprising the steps of receiving one or more input parameters (column 4, line 56 to column 5, line 8 and column 19, lines 16-33), defining a plurality of processing elements based upon said received one or more input parameters (column 18, line 53 to column 19, line 33, column 19, lines 38-68 and column 20, lines 43-48) and connecting said plurality of processing elements to define a processing web (column 4, lines 14-56 and Figure 1), wherein at least one of said plurality of processing elements requests processing from an upstream one of said plurality of processing elements so that upon said request, the upstream processing element performs said requested processing to provide required data to the at least one processing element (i.e. the display controller requests the memory management unit "14" to process memory access communications to control access

to memory banks in the waveform memory "16" and returns the required data, as part of a read access communication, from waveform memory back to the display controller) (column 5, lines 9-29 and 51-65 and Figure 1).

With respect to claim 45, Batson discloses a graphical processing web defining processing in a digital oscilloscope processing apparatus (column 2, lines 13-14), comprising a plurality of processing elements that are defined based upon one or more received input parameters (column 18, line 53 to column 19, line 33, column 19, lines 38-68 and column 20, lines 43-48), each of said processing elements performing a discrete processing function (column 19, lines 16-33 and 47-68), and a plurality of connections between said plurality of processing elements to define a flow of information therebetween (column 4, lines 14-56 and Figure 1), wherein at least one of said plurality of processing elements requests processing from an upstream one of said plurality of processing elements so that upon said request, the upstream processing element performs said requested processing to provide a result from the processing to the at least one of the plurality of processing elements requesting the processing (i.e. the display controller requests the memory management unit "14" to process memory access communications to control access to memory banks in the waveform memory "16" and returns the required data, as part of a read access communication, from waveform memory back to the display controller) (column 5, lines 9-29 and 51-65 and Figure 1).

With respect to claim 47, Batson discloses a graphical processing web defining processing in a digital processing apparatus (column 2, lines 13-14), comprising a

plurality of processing elements that are defined based upon one or more received input parameters (column 18, line 53 to column 19, line 33, column 19, lines 38-68 and column 20, lines 43-48), each of said processing elements performing a discrete processing function (column 19, lines 16-33 and 47-68), and a plurality of connections between said plurality of processing elements to define a flow of information therebetween (column 4, lines 14-56 and Figure 1), wherein at least one of said plurality of processing elements requests processing from an upstream one of said plurality of said plurality of processing elements so that upon said request, the upstream processing element performs said requested processing to provide a result from the processing to the one of the plurality of processing elements requesting the processing (i.e. the display controller requests the memory management unit "14" to process memory access communications to control access to memory banks in the waveform memory "16" and returns the required data, as part of a read access communication, from waveform memory back to the display controller) (column 5, lines 9-29 and 51-65 and Figure 1).

With respect to claims 2 and 23, Batson discloses that at least two of said plurality of processing elements are updated at different speeds (column 20, lines 12-30).

With respect to claims 3 and 24, Batson discloses that a processing object controls the update of said at least two of said plurality of processing elements (column 20, lines 12-30).

With respect to claims 4 and 25, Batson discloses that one of said at least two of said plurality of processing elements operates at an acquisition speed and another of said at least two of said plurality of processing elements operates at a display speed, and wherein the acquisition speed is higher than the display speed (column 20, lines 12-30).

With respect to claims 5 and 26, Batson discloses that said at least two of said plurality of processing elements are idle when not updated (i.e. idle until an corresponding input changes) (column 20, lines 12-30).

With respect to claims 6 and 27, Batson discloses that one of said at least two of said plurality of processing elements is of a cumulative type running at a first speed (column 19, lines 27-33), and another of said at least two of said plurality of processing elements is of a non-cumulative type running at a second speed (column 19, lines 53-60), and wherein the first speed is higher than the second speed (column 20, lines 12-30).

With respect to claims 11, 32, and 48, Batson discloses that one of said plurality of processing elements requests data and processing from an upstream source when data is requested from it by a downstream processing element (i.e. the display controller requests the memory management unit "14" to process memory access communications to control access to memory banks in the waveform memory "16" and returns the required data, as part of a read access communication, from waveform memory back to the display controller) (column 5, lines 9-29 and 51-65 and Figure 1).

With respect to claims 44, 46, and 49, Batson discloses that the upstream one of said plurality of processing elements transmits the requested data as the result of processing to the at least one of the plurality of processing elements requesting data and processing therefrom (i.e. display controller) without an intervening buffer (column 5, lines 9-29 and 51-65 and Figure 1).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Batson in view of U.S. Patent No. 5,736,971 to Shirai.

As noted above, Batson teaches many of the features of the claimed invention, and while the invention of Batson does disclose updating processing elements based upon a request with at least one processing element, such as the display controller, receiving at least one input and producing at least zero outputs, Batson does not explicitly describe the use of pins.

Shirai teaches a method and apparatus for increasing resolution of a computer graphics display including a display controller for connection to a CRT (column 5,

lines 12-15) that receives data inputs through at least one input pin (i.e. pin connector CN1) (column 5, lines 34-45), produces outputs through at least one output pin (i.e. pin connectors CN2-CN4) (column 5, lines 4-6), and receives controlling instructions through a processor at a pin (i.e. pin connector CN1) (column 4, lines 43-49).

It would have been obvious to one having ordinary skill in the art to modify the invention of Batson to include specifying that the processing element uses pins, as taught by Shirai, because the invention of Batson does teach the application of the processing device that receives data, outputs data, and receives controller signals from a processor for update indications, but does not give the specifics as to how the data is received (i.e. through pins), and Shirai suggests a corresponding well-known structure applicable to carry out the invention of Batson that further allows synchronizing adjustments to improve processing (column 2, lines 45-50).

Response to Arguments

8. Applicant's arguments with respect to claims 2-6, 11, 13, 23-27, 32, and 43-49 have been considered but are moot in view of the new ground(s) of rejection.

The following arguments, however, are noted:

Applicant first argues:

> Thus, independent claim 43 now recites "wherein at least one of said plurality of processing elements requests processing from an upstream one of said plurality of processing elements so that upon said request, the upstream processing element performs said requested processing to provide required data to the at least one requesting processing element." This recitation makes it clear that it is upstream processing, performed in response to a downstream request, that provides the requested data. Independent claims 45 and 47 similarly recite

"wherein at least one of said plurality of processing elements requests processing from an upstream one of said plurality of processing elements so that upon said request, the upstream processing element performs said requested processing to provide a result from the processing to the at least one of the plurality of processing elements requesting the processing." This recitation provides for the request to be for upstream processing, the result thereof being passed downstream to the requestor.

In contrast, the portions of Baston relied upon by the Examiner show no such processing. Rather a request to retrieve data from a buffer is shown. Indeed, as noted by Applicants in their application as filed, and as additionally presented in at least, for example dependent claims 46 and 49, the present inventions allows for the omission of intermediate buffers as processing of upstream processing elements only takes place upon a request from a downstream processing element when it needs input information. Applicants would suggest that merely retrieving data from a storage location does not constitute processing as claimed in the present invention.

The Examiner asserts that Batson specifically states:

As can be seen from the foregoing description of the digital oscilloscope system 10 of FIG. 1, the digitizer 12, the display controller 18 and the microprocessor 24 all have competing demands for access to the waveform memory 16. For example at the same time digitizer 12 wishes to transmit digitized waveform data for storage in the waveform memory 16, the microprocessor 24 may want to transmit processed waveform data for storage in the memory, and the display controller 18 may want to read data out of the memory. These competing demands for memory access can limit the real time performance of the oscilloscope in terms of its ability to rapidly generate, store and display waveform data. Memory management unit 14 is provided to arbitrate these competing demands for memory access from digitizer 12, display controller 18, and microprocessor 24. Moreover, memory 16 and MMU 14 are adapted to permit concurrent access to the waveform memory 16 by any two of these devices during a single memory access cycle, thereby improving the real time performance of the oscilloscope. (column 5, lines 9-29)

When two data processing devices attempt to write data into the waveform memory 16 at the same time, the MMU 14 controls access to the even and odd banks such that during one memory access cycle, a first data processing device writes to the odd bank 16a, while a second data processing device writes to the even bank 16b and during a next memory access cycle, the first data processing device writes to the even bank while the second data processing device writes to the odd bank. In this arrangement each data processing device is able to write a

> data sequence into (or read a data sequence out of) memory 16 without substantially interfering with the rate at which the other device writes a data sequence into (or reads a data sequence out of) the memory. (column 5, lines 51-65)

As can be seen by these cited sections, the invention of Batson describes, *inter alia*, a display controller processing element (downstream) that requests reading data from banks of a memory through a memory management unit (upstream) by sending an access communication. If the access communication for retrieving data by the display controller is made at the same time as an access communication from another processing element, such as a digitizer or microprocessor, the memory management unit processes the access communications in order to generate alternating access commands. The resulting data to be read is then provided from the memory to the display controller by the memory management unit generating a data signal.

Therefore, the Examiner asserts that the invention of Batson meets the limitation of "wherein at least one of said plurality of processing elements requests processing from an upstream one of said plurality of processing elements so that upon said request, the upstream processing element performs said requested processing to provide a result from the processing to the at least one of the plurality of processing elements requesting the processing."

The Examiner also asserts that when there are no competing requests for data, the memory management unit at least processes a received "AVAIL" signal and in response places data on a data bun and transmits a "SENT" signal, specifically:

> When the display controller 18 is free to receive waveform, graphics or message data stored in memory 16, it transmits an AVAIL signal to the MMU 14. Thereafter, when the MMU 14 is ready to transmit a 16 bit data word to the display controller 18, it places the data in memory on a data bus to the display controller and transmits a SENT signal to the display controller causing the display controller to read the data on the bus. (column 7, lines 47-55)

Applicant then argues:

> Claim 13 depends from independent claim 1 and is therefore allowable for this reason alone. Furthermore, the present invention is directed to a graphical representation of a processing web. Shirai describes a hardware system. Similar to the arguments made above with respect to independent claims 45 and 47, Applicants are at a loss to understand how mention of a hardware connector including pins (which is clearly well known) has any bearing on the use of the claimed pins in a graphical representation of the claimed processing web. Because Shirai fails to teach the claimed invention, and indeed fails to cure the defects noted above with respect to Baston, for this additional reason, applicants respectfully request that the rejection of claim 13 under 35 USC 103(a) be withdrawn.

The Examiner asserts that claim 13, which depends from independent claim 43, contains no mention of any graphical aspects. Therefore, Applicant's arguments that Shirai's hardware connectors are not applicable to a graphical system are not persuasive.

The Examiner also asserts that Shirai's illustration of a hardware system including pins could still be applicable to a graphical system that is trying to emulate and/or program a hardware system as the hardware connection would need to be represented in the graphical system.

The Examiner further asserts that the recitation of "graphical" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of

a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Additionally, since the preamble of some of the claims have only been modified to recite "A graphical processing web defining processing in a digital oscilloscope processing apparatus", wherein the body of the claims do not further define any "graphical" aspects, and the invention of Batson discloses a processing web defining processing in a digital oscilloscope processing apparatus wherein the processing web is used to perform graphical processing for displaying data in an oscilloscope, the invention of Batson can correctly be interpreted as meeting the limitation for a "graphical processing web".

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure:

U.S. Patent No. 5,301,336 to Kodosky teaches a method for configuring and performing processing in an instrument comprising the steps of receiving one or more input signals by the instrument (column 9, lines 44-47, column 10, lines 54-59 and column 15, lines 4-20), receiving one or more input parameters by the instrument (column 32, lines 47-50), defining a set of instructions input by a user to

be associated with one or more processing elements of the instrument, based upon said one or more input parameters (column 9, lines 58-64 and column 32, line 48 to column 33, line 16), to enable said processing elements to carry out said instructions and perform processing on the received input signals within the instrument upon application of the associated processing element (column 33, line 66 to column 34, line 13), assigning a graphical representative for each said processing element (column 32, lines 5-7 and column 33, lines 19-25), coupling one or more of the received input signals to one or more processing element graphical representatives (column 31, lines 13-18 and column 34, lines 2-13), and connecting respective ones of said processing element graphical representatives to define and graphically depict a processing web for performing corresponding processing on said one or more received input signals within said instrument (column 34, lines 1-16 and Figure 74).

U.S. Patent No. 6,570, 592 to Sajdak et al. teaches a system and method for specifying trigger condition of a signal measurement system using graphical elements on a graphical user interface.

U.S. Patent No. 5,953,009 to Alexander teaches a graphical system and method for invoking measurements in a signal measurement system.

National Instruments, "Computer-Based Instruments: NI 5911 User Manual Digital Oscilloscope for PCI", teaches a digital oscilloscope programmed by means of graphical representatives of processing elements.

National Instruments, "NI-SCOPE Instrument Driver Quick Reference Guide: Easy Programming for National Instruments Oscilloscopes", teaches graphical

representatives of processing elements for use in programming a digital oscilloscope.

U.S. Patent No. 5,920,479 to Sojoodi et al. discloses a method for configuring and performing processing in a digital oscilloscope (column 1, lines 60-67) comprising the steps of receiving one or more input signals by the digital oscilloscope (column 3, lines 10-21 and column 13, lines 51-67), receiving one or more input parameters by the digital oscilloscope (column 19, lines 48-59), selecting a set of instructions by a user (column 15, lines 11-15, column 17, lines 30-54, and column 25, lines 46-56) to be associated with one or more processing elements of the digital oscilloscope, based upon said one or more input parameters, to enable said processing elements to carry out said instructions and perform processing on the received input signals within the digital oscilloscope upon application of the associated processing element (column 10, lines 59-64), assigning a graphical representative for each said processing element (column 13, lines 51-67), coupling one or more of the received input signals to one or more processing element graphical representatives (column 13, lines 51-67), and connecting respective ones of said processing element graphical representatives to define and graphically depict a processing web for performing corresponding processing on said one or more received input signals within said digital oscilloscope (column 17, line 55 to column 18, line 32).

U.S. Patent No. 5,668,469 to Natori et al. teaches a digital oscilloscope using a color plane display device and data display method comprising a plurality of

processing elements, including acquisition devices and display devices, (Figure 1), wherein the data read out of a display memory using a display controller is in synchronization with the other processing elements (abstract and column 4, line 42 to column 5, line 14).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (571)272-2226. The examiner can normally be reached on Monday through Friday, 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571)272-2216. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeffrey R. West
Examiner – AU 2857

March 18, 2007